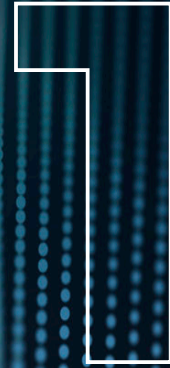




SCR1 MICRO- CONTROLLER CORE



OVERVIEW

The SCR1 core is an open-source, RISC-V-compatible, 32-bit, entry-level microcontroller-class core, designed by Syntacore for general-purpose, deeply embedded applications and control systems.

This compact industry-grade IP core is based on the Harvard architecture with separate instruction and data buses and includes an in-order 4-stage pipeline, an IPIC unit, a TCM, industry-standard AXI4/AHB-Lite and JTAG or cJTAG* interfaces. SCR1 is fully compliant with the RISC-V open instruction set architecture (ISA) defined by RISC-V International. The core can be configured for a very small area starting from 10k gates and is open-sourced under the permissive SHL license, which allows commercial use.

The core comes with pre-configured software tools and is ready for use out-of-the-box for commercial and educational purposes.

* Available upon request



Figure 1 - Block diagram of the SCR1 processor

ADVANTAGES

- [Open-source](#)
- Compact size
- Low power-optimized
- Flexibility and customization
- High performance
- Suitable for educational purposes

SCR1 MICROCONTROLLER CORE

TECHNICAL SPECIFICATION

Feature	Description
ISA Support	RV32I/E[MC], Integer Multiplication and Division [M], Compressed Instructions [C] — optional
Execution Privilege Levels	Machine mode
Pipeline	In-order 2 – 4 stage pipeline (integer)
Hardware Multiplier/Divider	Speed-optimized/area-optimized
Optional Tightly-Coupled Memory (TCM)	I/D-shared, configurable: size - up to 64KB
Interrupt Support	IPIC - up to 16 interrupt lines, interrupt priority levels support
Embedded 64-bit RTC timer	Machine-mode timer interrupt support
Software Interrupts	Machine-mode software interrupt support
Low Power Management	Clock-gating support, power-gating support (coarse-grain power domain control, core-level UPF provided for low-power aware simulation and implementation), WFI (Wait For Interrupt) scheme to enter a sleep mode
Optional Debug Unit	JTAG/cJTAG-compliant interface, 2 hardware breakpoints, software breakpoints support
Advanced Performance Monitoring	2 performance counters
Bus Interfaces	Master AXI4 or AHB-Lite external memory interfaces

SCR1 MICROCONTROLLER CORE

BLOCK DIAGRAM

SCR1 has functional blocks included in the base configuration by default and optional blocks that can be added upon request during the development stage.

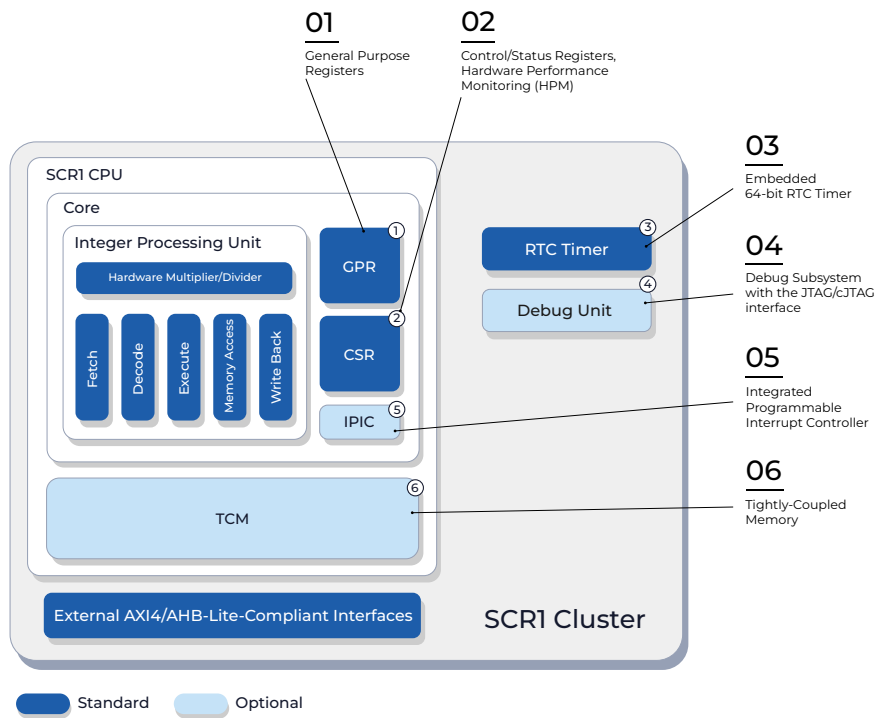


Figure 2 - SCR1 processor components

SCR1 MICROCONTROLLER CORE

CONFIGURATION OPTIONS

The SCR1 core platform offers wide customization possibilities with a default set of features that can be configured to meet your requirements.

Feature	Description
Instruction Set	RV32(I/IM/IMC/E/EM/EMC)
Hardware Multiplier/Divider	Speed-optimized/area-optimized according to requirements (iterative or pipelined configuration depending on frequency and performance requirements)
Optional Tightly-Coupled Memory (TCM)	4KB to 64KB
Interrupt Support	IPIC — up to 16 interrupt lines, interrupt priority levels support
Bus Interfaces	Master AXI with 32-bit data Master AHB-Lite with 32-bit data
Optional Debug Unit	Debug subsystem with the JTAG/cJTAG interface

SCR1 MICROCONTROLLER CORE



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INSTRUCTION SET

Default

I/E: Base/Reduced Base Integer,

Zicsr: Control and Status Register Instructions,

Zifencei: Instruction-Fetch Fence*

Optional

M: Integer Multiplication and Division,

C: Compressed Instructions

RV32/E Base Integer/Reduced Base Integer, CSR, Memory Ordering, and Custom Instructions								
BEQ	XOR	LB	SB	SLL	ADD	LWU	SRAIW	
BNE	XORI	LH	SH	SLLI	ADDI	LD	ADDW	
BLT	OR	LBU	SW	SRL	SUB	SD	SUBW	
BGE	ORI	LHU	SLT	SRLI	LUI	SLLI	SLLW	
BLTU	AND	LW	SLTI	SRA	AUIPC	SRLI	SRLW	
BGEU	ANDI	FENCE	SLTU	SRAI	ECALL	SRAI	SRAW	
JAL	JALR	FENCEJ	SLTIU	WFI	EBREAK	ADDIW		
CSRRLW	CSRRC	CSRRSI	SFENCE.VMA	SRET	MRET	SLLIW		
CSRRS	CSRRWI	CSRRCI	CLFLUSH**	CLINV**	CLLOCK**	SRLIW		
RV32M/64M Integer Multiplication and Division								
MUL	MULHSU	DIV	REM			MULW	DIVUW	REMUW
MULH	MULHU	DIVU	REMU			DIVW	REMW	
RV32C/64C Compressed Instructions								
CMV	CLW	C.SW	C.BEQZ	C.ADD	C.AND	CLD	C.SDSP	
CLI	CLWSP	C.SWSP	C.BNEZ	C.ADDI	C.ANDI	CLDSP		
CLUI	C.FLW	C.FSW	CJ	C.ADDI16SP	C.OR	C.ADDW		
C.SLLI	C.FLWSP	C.FSWSP	CJR	C.ADDI4SPN	C.XOR	C.ADDIW		
CSRAI	C.FLD	C.FSD	CJAL	C.SUB	C.EBREAK	C.SUBW		
CSRLI	C.FLDSWP	C.FSDSP	CJALR	C.NOP	...	C.SD		
RV32/64A Atomic Instructions								
LR.W	AMOXOR.W	AMOMAX.W				LR.D	AMOXOR.D	AMOMAX.D
SC.W	AMOAND.W	AMOMINU.W				SC.D	AMOAND.D	AMOMINU.D
AMOSWAP.W	AMOOR.W	AMOMAXU.W				AMOSWAP.D	AMOOR.D	AMOMAXU.D
AMOADD.W	AMOMIN.W					AMOADD.D	AMOMIN.D	
RV32/64F Single-Precision Floating-Point								
FLW	FNADD.S	FSQRT.S	FCVT.WS	FLE.S	FSGNJXS	FCVT.LS		
FSW	FADD.S	FSGNJ.S	FCVT.WUS	FCLASS.S		FCVT.LUS		
FMADD.S	F.SUB.S	FSGNJ.N.S	FMV.XS	FCVT.SW		FCVT.SL		
FMSUB.S	FMUL.S	FMIN.S	FEQ.S	FCVT.SWU		FCVT.SLU		
FNMSUB.S	FDIV.S	FMAX.S	FLT.S	FMV.WX				
RV32/64D Double-Precision Floating-Point								
FLD	FNADD.D	FSQRT.D	FMAX.D	FLE.D	FCVT.D.WU	FCVT.LD	FMV.DX	
FSD	FADD.D	FSGNJ.D	FCVT.SD	FCLASS.D		FCVT.LUD		
FMADD.D	F.SUB.D	FSGNJ.N.D	FCVT.DS	FCVT.WD		FMV.XD		
FMSUB.D	FMUL.D	FSGNJ.X.D	FEQ.D	FCVT.WUD		FCVT.DL		
FNMSUB.D	FDIV.D	FMIN.D	FLT.D	FCVT.DW		FCVT.DLU		
RV32/64B Bit Manipulation								
CLMUL**	CTZ	MAX	ORCB	BEXTI	BINVI	ADD.UW	CTZW	SHADD.UW
CLMULH**	SH2ADD	MAXU	SEXT.B	ROR	ANDN	SH2ADD.UW	RORIW	RORW
CLMULR**	BEXTI	MIN	SEXT.H	RORI	ORN	SH3ADD.UW	CPOPW	
CPOP	SH3ADD	MINU	ZEXT.H	BEXT	XNOR	SLLI.UW	CLZW	
SHIADD	ORC	REV8	ROL	BINV	..	ZEXT.H	ROLW	
RV32/64K Scalar Cryptography								
SHA256SIG0	SHA256SUM1	SM4ED	AES32DSMI	SHA512SIG0L	SHA512SUM0R	SHA512SIG1	AE564DS	AE565IM
SHA256SIG1	SM3P0	SM4KS	AES32ESI	SHA512SIG1H	SHA512SUM1R	SHA512SUM0	AE564DSM	AE564KSLI
SHA256SUM0	SM3P1	AES32DSI	SHA512SIG0H	SHA512SIG1L	AES32ESMI	SHA512SUM1	AE564ES	..
RV32/RV64						RV64		
RV64V Vector Operations								
VSETVLI	VMAXU	VSLIDEUP	VREDXOR	VASUBU	VFMIN	VFSGNJX	VSBC	VMSLT
VADD	VMAX	VRGATHEREII6	VREDMINU	VASUB	VFREDMIN	VSLIDEIUP	VMSBC	VMSLEU
VASUB	VAND	VSLIDEIDOWN	VREDMIN	VFADD	VFMAX	VSLIDEIDOWN	VMERGE	VMSLE
VRSUB	VOR	VREDSUM	VREDMAXU	VFREDUSUM	VFREDMAX	VFSLIDEUP1	VMSEQ	VMSTGJ
VMINU	VXOR	VREDAND	VREDMAX	VFSUB	VFSGNJ	VADC	VMSNE	VMSTG
VMIN	VRGATHER	VREDOR	VADDU	VFREDOSUM	VFSGNJN	VMADC	VMSLTU	..

SCR1
SCR3, SCR4, SCR5, SCR6, SCR7
SCR9B

Figure 3 - SCR1 instruction set

*For a complete list of supported instructions, please refer to the SCR1 Instruction Set Manual

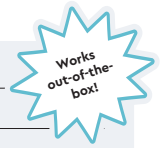
SCR1 MICROCONTROLLER CORE


SOFTWARE

Syntacore develops and supports a wide range of tools optimized for SCR cores. This includes a ready-to-use package for software development ([Syntacore Development Toolkit](#)), a pre-built FPGA SDK, system software and detailed documentation. In addition, Syntacore provides an extensive support for third-party debugging hardware and software.

Syntacore Development Toolkit:

- Pre-built, tested and ready-to-use bundle
- Pre-configured and optimized for SCR cores
- Industry-quality toolchains support (GCC and LLVM)
- Support and regular release cycles
- Pre-configured OCD and GDB with Python scripts



Software	Description
Syntacore Development Toolkit 	
IDE	Visual Studio Code plugin Eclipse
Toolchain	GCC with binutils and Newlib libraries clang/LLVM compiler
Debuggers	GNU GDB OpenOCD
Simulator	QEMU
Software Examples	Sample applications and benchmarks HAL and BSP
OS	FreeRTOS/(RTEMS/ Zephyr)*
Bootloader and Firmware	First-stage bootloader
Documentation	SDK User Guide, Tools Guide (IDE, CLI)
Third-Party Tools	
SEGGER	Probe: J-Link Ultra+ IDE: Embedded Studio
Lauterbach	Probes: PowerDebug PowerTrace Debugger: Trace32
Ashling	Probe: Opella-XD IDE: RiscFree™
Digilent	Probe: JTAG-HS2
Olimex	Probes: ARM-USB-TINY-H ARM-USB-OCD-H

*Downloaded separately



SCRI MICROCONTROLLER CORE



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DEVELOPMENT BOARDS

The SCRI product package includes a ready-to-use FPGA development suite that features comprehensive documentation and pre-configured FPGA images. The package provides developers with an easy way to start working on their SCRI-based projects.

Supported FPGAs*

Manufacturer	Model
Digilent	ARTY A7-100T
AMD/XILINX	AMD Virtex UltraScale+ FPGA VCU118
Intel	Arria V GX
	Arria 10 GX

FPGA Resources Utilization**

FPGA	Configuration
	SCRI TCM 64KB
Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit 1182 240 LUTs / 2160 BRAM	0.52%/0.74%
Arty Nexys A7 (100T) 63 400 LUTs / 135 BRAM	9.88%/11.85%
Arria® 10 GX FPGA Development Kit 427 200 ALMs 55 562 240 RAM bits	0.89%/1.89%
Arria V GX FPGA Starter Kit 136 880 ALM 17 674 240 RAM bits	2.82%/5.94%

*Standard FPGA development boards supported by default. Customer FPGA images can be considered upon request.

**FPGA resources utilization by a RISC-V CPU cluster (base configuration).

SCR1 MICROCONTROLLER CORE

PRODUCT PACKAGE

The SCR1 product package includes:

Component	Contents
RISC-V Compatible Core	<ul style="list-style-type: none">• System Verilog RTL source code
Syntacore Development Toolkit (downloaded separately)	<ul style="list-style-type: none">• Toolchains• OS and bootloaders• IDEs• Debuggers• Simulator• Software example projects, HAL and BSP
FPGA-based SDK	<ul style="list-style-type: none">• Sample FPGA projects• Pre-build FPGA images
Tests and Scripts for Simulation	<ul style="list-style-type: none">• Verification test suite for pre-silicon (RTL simulation-based)• Verilator simulation support
Comprehensive Documentation	<ul style="list-style-type: none">• User Manual (quick start guide)• External Architecture Specification (EAS)• SDK User Guide• Tools Guide

Full RTL and supplementary collateral are available from the [github repository](#).

SCR1 MICROCONTROLLER CORE

POWER, PERFORMANCE, AND AREA

Performance*, per MHz	Dhrystone	-O2	Configuration	
			32-bit	
		best**	1.55	
		best**	3.15	
	Coremark	best***	3.05	
Area, kGates			10.36	

Conditions: *Dhrystone 2.1, Coremark 1.0, LLVM-20-sc, run from TCM, **LLVM-20-sc Obest with LTO, ***LLVM-20-sc Obest with ground rules, configuration - RV32IM, 3-stage pipeline, TCM 32KB

Configuration	90LP		28HPC	
	Area	Power	Area	Power
MIN*	0.027 mm ²	5.82 uW/MHz	0.004 mm ²	1.40 uW/MHz
BASE**	0.07 mm ²	10.18 uW/MHz	0.010 mm ²	2.38 uW/MHz
MAX***	0.091 mm ²	9.96 uW/MHz	0.013 mm ²	2.29 uW/MHz

Configuration	Max Frequency (9-TRACK, LVT, TYPICAL 1.2V, 25°C) W/O DFT	Max Frequency (28HPC+, 12-TRACK, LVT, TYPICAL 0.9V, 25°C)
	MIN*	150+ MHz
BASE**	250+ MHz	1100+ MHz
MAX***	300+ MHz	1200+ MHz

Conditions:

Area 90LP - 9-track, LVT, typical 1.2V, 25°C @50MHz, without DFT, core logic only
 Area 28HPC - 9-track, LVT, typical 0.9V, 25°C @100MHz, without DFT, core logic only
 Power - Measured at a post phys synthesis gate-level netlist,
 Dhrystone 2.1 run from TCM, 10 last iterations of 500,
 90LP - 9-track, LVT, worst 1.08V, 125°C @50MHz, without DFT, core logic only
 28HPC - 9-track, HVT, typical 0.9V, 25°C @100MHz, without DFT, core logic only

Configurations:

*RV32EC, TCM 32KB, no Debug Unit, no IPIC, no HW Multiplier, 1 IRQ
 **RV32IC, TCM 32KB, a full feature set configuration
 ***RV32IMC, TCM 32KB, a full feature set configuration

CONTACT DETAILS

To learn more about the SCR1 core,
 contact Syntacore or visit the web:

<https://syntacore.com>

sales@syntacore.com



NOTES

DS_SCR1 - v2